REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Office Action and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Status of Claims

Claims 1 – 11, 13, 16, 18, 20 –27, 29, 30, 41 and 53 are pending in the application.

Claims 33 – 40 have been withdrawn from consideration.

Claims 12, 14, 15, 17, 19, 28, 31, 32 and 42-52 are canceled without prejudice.

Claims 1-10, 13, 16, 18, 20 – 23, 29, 41 and 53 are amended.

Applicant respectfully assert that the amendments to these claims do not add new matter.

35 U.S.C. 112 Rejections

The Office Action rejected claims 1-19 and 42-44 under 35 U.S.C. 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claims 1–11, 13, 16, and 18, have been amended to remove any potentially indefinite language and, thereby, to overcome the above rejections under 35 U.S.C. 112. Claims 12, 14, 15, 17, 19 and 42 - 44 have been canceled and, therefore, the rejection of these claims is now moot. Furthermore, Applicant respectfully submits that the claims have been amended to make the claim language clear and concise.

In the view of the above amendments, Applicant respectfully asserts that claims 1-11, 13, 16 and 18, as amended, are proper under 35 U.S.C 112 and request that the indefiniteness rejections be withdrawn.

35 U.S.C. § 103 Rejections

The Office Action rejected claims 1–32 and 41-53 under 35 U.S.C. 103(a) as being unpatentable over Fettweis or Schwartz in view of van der Wal.

In view of the above amendments and the following remarks. Applicant respectfully requests that this rejection be withdrawn.

Claims 12, 14, 15, 17, 19, 28, 31, 32, 42 - 52 have been canceled, and thus, Applicant respectfully submits that the rejection of these claims is now moot and does not need to be addressed.

As to the non-canceled rejected claims 1-11, 13, 16, 18, 20-27, 29, 30, 41 and 53, it is well established that an obviousness rejection requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (MPEP 2142).

Applicant respectfully asserts that neither Fettweis or Schwartz nor van der Wal, alone or in combination, teach or suggest the subject matter recited by claims 1–11, 13, 16, 18, 20 –27, 29, 30, 41 and 53, as amended.

Specifically, neither Fettweis or Schwartz nor van der Wal, alone or in combination, discloses, teaches or suggests an adapter of a wave digital filter including "a controlled gate to delay the propagation of a value into or within the adapter based on the validity of an input signal value", as recited by amended independent claim 1.

Accordingly, Applicant respectfully asserts that a *prima facie* case of obviousness of amended claim 1 in view of the cited references cannot be established, and Applicant respectfully requests that the rejection be withdrawn.

Since claims 2–11, 13, 16, 18 and 41 are dependent, directly or indirectly, from independent claim 1, Applicant respectfully requests that the rejection of these claims be withdrawn for at least the same reason.

Independent claim 20, as amended, recites, among other things, "an adapter having a delay unit to delay the propagation of a first value into a first input of the adapter such that the first value is received substantially concurrently with a second value at a second input of the adapter". Applicant respectfully assert that neither Fettweis or Schwartz nor van der Wal, alone or in combination, teaches or suggests "an adapter having a delay unit" as recited in amended claim 20. Accordingly, Applicant respectfully assert that a *prima facie* case of obviousness of amended claim 20 in view of the cited references cannot be established, and Applicant respectfully requests that the rejection of claim 20 be withdrawn.

Since claims 21 and 22 are dependent from independent claim 20, Applicant respectfully requests that the rejection of these claims be withdrawn for at least the same reason.

Independent claim 23, as amended, recites, among other things, "delaying propagation of an input signal value into a memoryless adapter of a wave digital filter until the input signal value is valid; and enabling the memoryless adapter to calculate the valid value."

Applicant respectfully asserts that neither Fettweis or Schwartz nor van der Wal, alone or in combination, teaches or suggests "delaying propagation of an input signal value into a memoryless adapter of a wave digital filter until the input signal value is valid; and enabling the memoryless adapter to calculate the valid value" as recited in amended by independent claim 23.

Accordingly, Applicant respectfully assert that a *prima facie* case of obviousness of claim 23 in view of the cited references cannot be established, and Applicant respectfully requests that the rejection of claim 23 be withdrawn.

Since claims 24-27 are dependent from claim 23, Applicant respectfully requested that the rejection of these claims be withdrawn for at least the same reason.

Applicant further asserts that neither Fettweis or Schwartz nor van der Wal, alone or in combination, teaches or suggests "delaying the value at the first input until a valid value is received on a second input of the adapter; and enabling the adaptor to calculate the delayed value " as recited in amended claim 29.

Accordingly, Applicant respectfully asserts that a *prima facie* case of obviousness of claim 29 over the cited references cannot be established, and Applicant respectfully requests that the rejection of claim 29 be withdrawn.

Since claims 30 1s dependent from claim 29, Applicant respectfully requested that the rejection of this claim be withdrawn for at least the same reason.

Additionally, Applicant respectfully asserts that neither Fettweis or Schwartz nor van der Wal, alone or in combination, teaches or suggests "a controlled gate to control the propagation of a value generated by a first adapter into a second adapter based on the validity of the value." as recited in amended claim 53.

Accordingly, Applicant respectfully assert that a *prima facie* case of obviousness of amended claim 53 in view of the cited references cannot be established and Applicant respectfully requests that the rejection of claim 53 be withdrawn.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Favorable reconsideration and allowance of the application are thus respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims, the following changes were made:

1. (Twice amended) A wave digital filter, comprising:

[a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and]

an adapter having a [at least one] controlled gate [which] to delay[s] the propagation of a value into or within [of at least one of] the adapter based on the validity of an input signal value. [s, without affecting a result value provide by the wave digital filter].

2. (Once amended) A wave digital filter according to claim 1, wherein the [at least one] controlled gate of the adapter comprises [at least one] a latch.

3. (Once amended) A wave digital filter according to claim 1, wherein the [at least one] controlled gate of the adapter comprises [at least one] a strobe gate.

4. (Once amended) A wave digital filter according to claim 1, wherein the [at least one] controlled gate of the adapter is opened when the value to be delayed by the controlled gate is expected to be valid.

5. (Once amended) A wave digital filter according to claim 1, wherein the value to be delayed by the [at least one] controlled gate of the adapter is one of two or more of values required [with other values for] to perform [ing] a function, and wherein the controlled gate is opened when [all the] the two or more values required [for] to perform[ing] the function are expected to be valid.

6. (Once amended) A wave digital filter according to claim 1, wherein the [at least one] controlled gate of the adapter is opened when substantially [all] the two or more values entering the [at least one of the] adapter[s] are expected to be valid.

7. (Once amended) A wave digital filter according to claim 1, comprising [at least one] a delay unit to [which] delay[s] the propagation of [a] the value into an input [of one] of the adapter[s] for a predetermined time period.

8. (Once amended) A wave digital filter according to claim 7, wherein the [at least one] delay unit comprises [at least one] said controlled gate.

9. (Once amended) A wave digital filter according to claim 7, wherein the [at least one] delay unit comprises [at least one] an uncontrolled delay element.

10. (Once amended) A wave digital filter according to claim 7, comprising two or more adapters wherein the [at least one] delay unit is able to delay[s] the propagation of the value such that the value enters [the] one of the two or more adapters substantially [concurrently] simultaneously with another value received by [the one] another adapter of the two or more adapters.

13. (Once amended) A wave digital filter according to claim 1, wherein [at least some of the plurality of] the adapter[s] comprises two or more ports [are three-port adapters].

16. (Once amended) A wave digital filter according to claim 1, wherein [each of the at least one of] the adapter[s into which propagation of values are delayed] comprises [at least one] a multiplier.

18. (Once amended) A wave digital filter according to claim 1, wherein the [plurality of] two or more adapters comprise [at least] two or more different types of adapters.

20. (Once amended) A wave digital filter, comprising:

[a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and]

an adapter having [at least one] a delay unit [which] to delay[s] the propagation of a first value into [at least one] a first input of [at least one of] the adapter[s] such that the first value is received substantially concurrently with a second value at [another] a second input of the adapter.

21. (Once amended) A wave digital filter according to claim 20, wherein the [at least one] delay unit comprises [a] said controlled gate.

22. (Once amended) A wave digital filter according to claim 20, wherein the [at least one] delay unit comprises an uncontrolled delay element.

23. (Once amended) A method [of filtering a signal using a wave digital filter,] comprising:

[providing an input which carries a value required for performing a calculation by a memoryless adapter of the wave digital filter;]

delaying propagation of an input signal value into a memoryless adapter of a wave digital filter[the input] until [its] the input signal value is valid; and

[providing] enabling the memoryless adapter to calculate the valid value [to the adapter].

29. (Once amended) A method [of filtering a signal using a wave digital filter,] comprising:

[providing a first input which carries a value required for performing a calculation by a memoryless adapter of the wave digital filter;]

delaying propagation of an input signal value [the value] on [the] a first input of a memoryless adapter until a valid value is received on a second input of the memoryless adapter; and

[providing] enabling the adaptor to calculate the delayed value [to the adapter].

41. (Once amended) A wave digital filter according to claim 1, wherein the [at least one] controlled gate is able to delay[s] the propagation of the value until a predetermined number of changes in the value occur.

53. (Once amended) A wave digital filter, comprising:

[a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and]

a [at least one] controlled gate [which] to [delays] control the propagation of a value generated by a first adapter[one of the adapters] [in]to a second [one of the] adapter[s] based on the validity of the value.